

CIR-S3SUSPM1308G

DDR3 SO-DIMM 1333MHz 8GB

Description

The CIR-S3SUSPM1308G is 1024M words X 64 bits, 2 ranks. Unbuffered Small Outline Dual In-Line Memory Module (SO-DIMM). DDR3 SDRAMs in Fine Ball Grid Array (FBGA) packages on a 204pin glass-epoxy substrate. Provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitable for easy interchange and addition.

Specifications

| | |
|------------------|-----------------|
| Density | 8GB |
| Pin Count | 204pin |
| Type | Unbuffered |
| Dimensions | 67.6mm x 30.0mm |
| ECC | Non-ECC |
| Component Config | 512M x 8 bit |
| Data Rate | 1333 MHz |
| CAS Latency | 9 |
| Voltage | 1.5V / 1.35V |
| PCB Layers | 8 |
| Operating Temp. | 0°C~+85°C |
| Module Ranks | Dual Rank |

Features

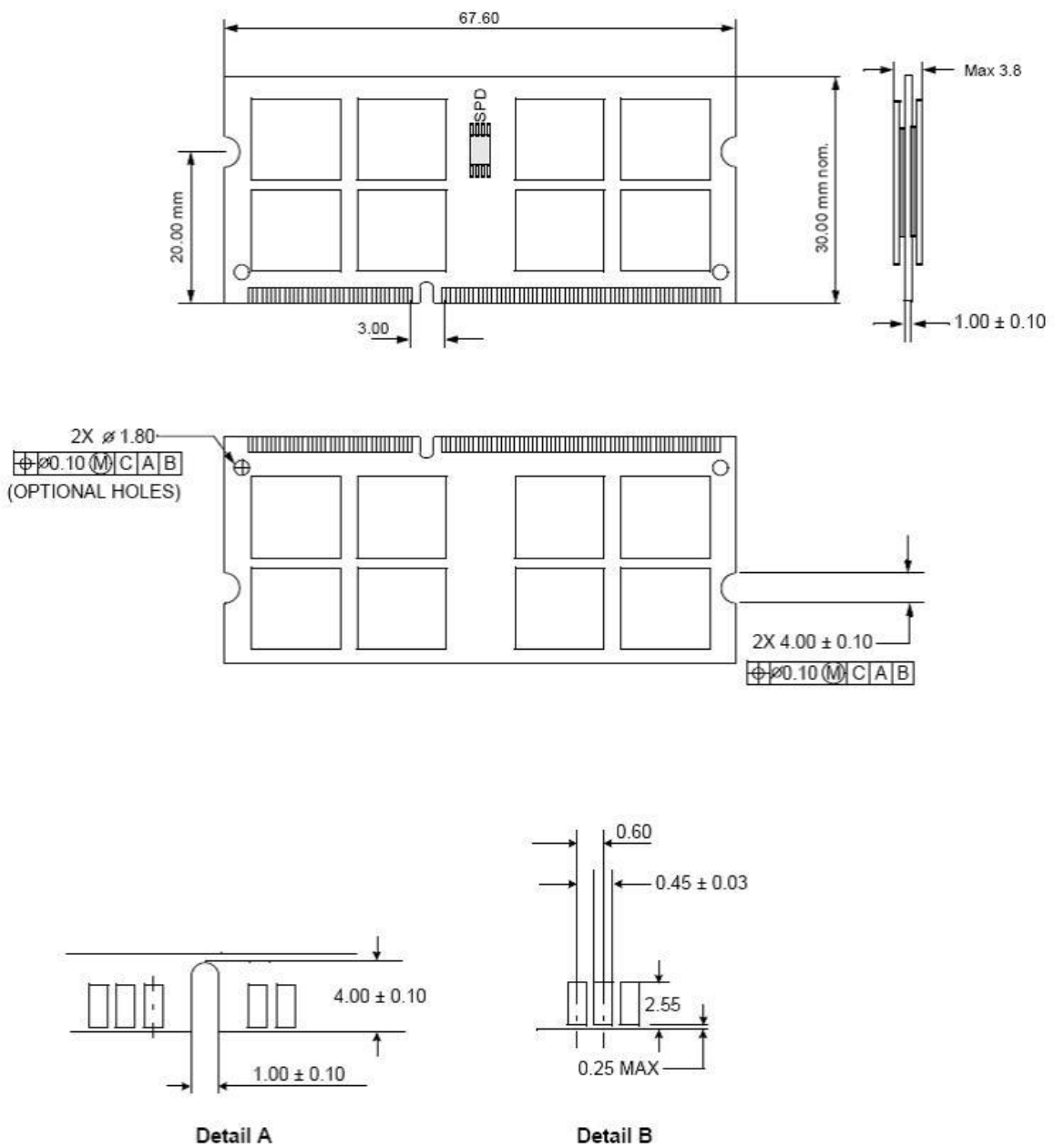
- Data rate:1333MHz
- RoHS compliant products.
- 204pin, Small outline dual in-line memory module (SO-DIMM)
- Power supply: VDD= 1.5V (1.425V to 1.575V) & VDD= 1.35V (1.283V to 1.45V)
- Programmable CAS Latency (CL): 6, 7, 8, 9 support
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- Serial presence detect with EEPROM
- 8 independent internal bank
- 8K refresh cycles /64ms
- On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- Programmable Additive Latency (Posted CAS) : 0, CL - 2, or CL - 1 clock
- Bi-directional Differential Data Strobe
- Burst Length: 4, 8
- 8 bit pre-fetch
- Average Refresh Period 7.8us at $0^{\circ}\text{C} \leq \text{TC} \leq 85^{\circ}\text{C}$
3.9us at $85^{\circ}\text{C} < \text{TC} \leq 95^{\circ}\text{C}$

Speed Grade

| Frequency Grade | Data Transfer Rate | CAS Latency Support | | | | CL-tRCD-tRP |
|-----------------|--------------------|---------------------|------|------|------|-------------|
| | | CL6 | CL7 | CL8 | CL9 | |
| DDR3-1333 | PC3-10600 | 800 | 1066 | 1066 | 1333 | 9-9-9 |

Package Dimensions

Unit: mm



Tolerances : ± 0.15 mm unless otherwise specified