CIR-W2SUMG8002G

DDR2 WIDE TEMP. SO-DIMM 800MHz 2GB

Description

The CIR-W2SUMG8002G is 256M words x 64 bits, 2 ranks DDRII SDRAM Small Outline Dual In-line Memory Module, mounting 16 pieces of 1GB bits DDRII SDRAM sealed in FBGA package. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 4 bits prefetch-pipelined architecture. Data strobe (DQS and /DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop(DLL) can be set enable or disable. This module provides high density mounting without utilizing surface mount technology. Decoupling capacitors are mounted beside each FBGA on the module board.

Specifications

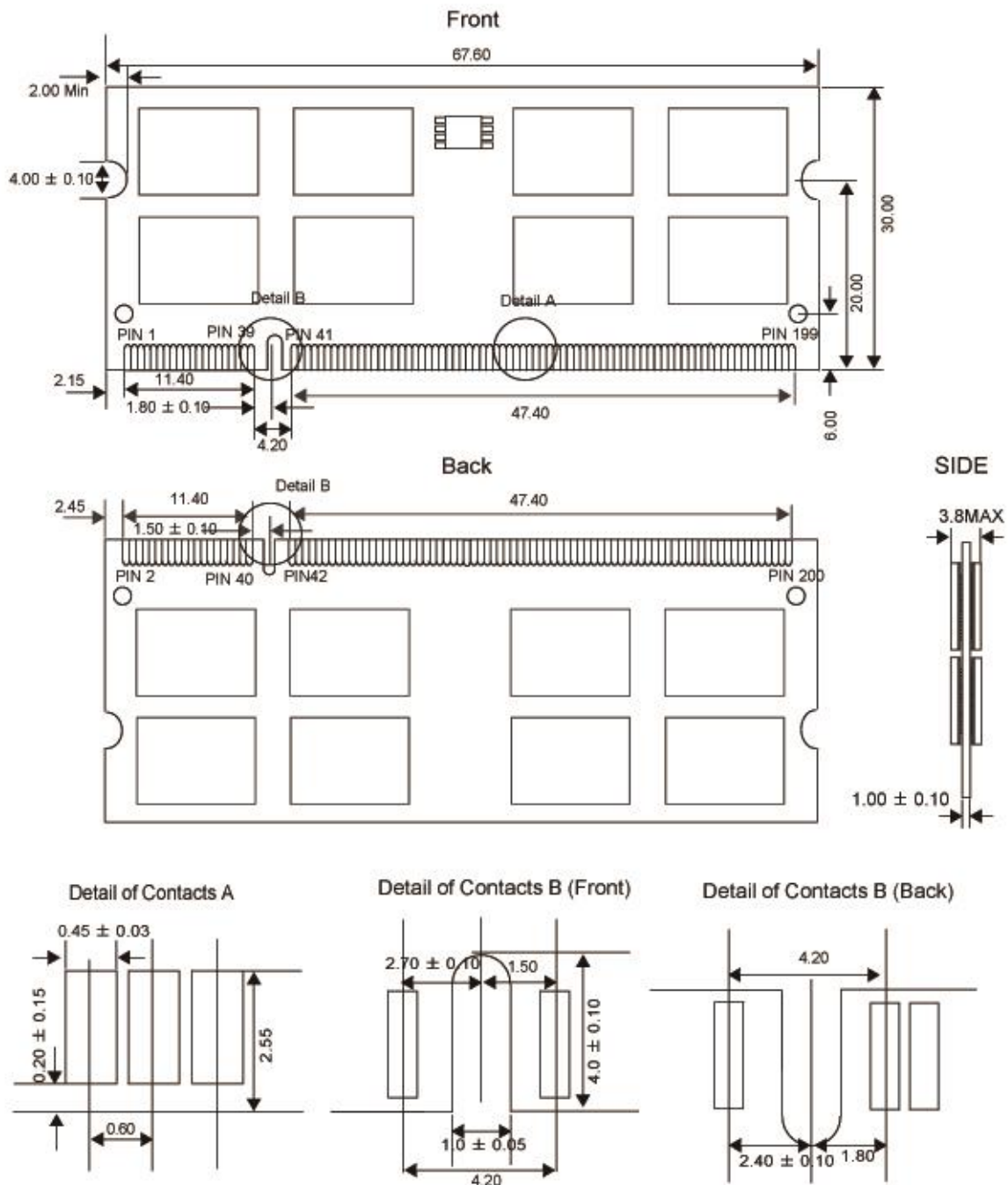|	
Density	2GB
Pin Count	200pin
Type	Unbuffered
Dimensions	67.6mm x 30.0mm
ECC	Non- ECC
Component Config	128M x 8 bit
Data Rate	800 MHz
CAS Latency	5
Voltage	1.8V
PCB Layers	8
Operating Temp.(Tcase)	-40°C~+95°C
Module Ranks	Dual Rank

Features

- JEDEC Standard 200-pin Dual In-Line Memory Module
- Inputs and Outputs are SSTL-18 compatible
- VDD=VDDQ= 1.8 Volt ± 0.1
- Differential clock input
- All inputs are sampled at the positive going edge of the system clock
- Bi-Directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge.
- Auto Refresh (CBR) and Self Refresh Modes support
- Serial Presence Detect with EEPROM
- Automatic and controlled precharge commands
- 14/10/2 Addressing (row/column/rank)-2GB
- Golden Contact
- DRAM Operation Temperature: -40°C ≤ TC ≤ +95°C
- Programmable Device Operation:
  Burst Type: Sequential or Inteleave
  Operation: Burst Read and Write
  Device CAS# Latency: 3,4,5
  Burst Length: 4, 8
- RoHS Compliant.

Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support			CL-tRCD-tRP
		CL3	CL4	CL5	
DDR2-800	PC2-6400	400	533	667/800	5-5-5

Package Dimensions

Unit: mm

Tolerances : ± 0.15mm unless otherwise specified