MEMXPRO

Make it Possible

Product Specification

MEMXPRO DDR4 VLP ECC UDIMM

Based on Hynix 8Gb 1Gx8 C-die

Revision V1.0

Compliance with

- JEDEC Standard 288-pin dual in-line memory module
- Intend for PC4-21300 application
- Backward compatible with PC4-19200
- Bi-Directional Differential Data Strobe
- 8 Bit pre-fetch
- 16 Internal banks
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- On-Die Termination (ODT)
- On-Board EEPROM
- Internal Vref DQ level generation is available
- RoHS and Halogen free
- Golden connector

Capacities

- 16GB 2Gx72 2Rank

Performance

- DDR4-2666 PC4-21300 CL19

DRAM Type

- DDR4 VLP ECC UDIMM

Temperature ranges

Operating:

- Standard: 0°C to 85°C
- Extended: -25°C to 85°C
- Industrial: -40°C to 85°C

Storage:

- -50°C to 100°C

Supply voltage

- VDD=VDDQ=1.2 Volt (TYP)
- VPP=2.5 Volt (TYP)
- VDDSPD=2.25V~3.6V

Form factor

- DDR4 288pin VLP ECC UDIMM

Shock &Vibration

- Shock: 1000G@1ms
- Vibration: 20 G

Certification and Compliance

- RoHs
- REACH

Revision History

Version	Description	Date
0.1	Internal release	2019/10/21
0.2	Part Number Recode	2019/10/21
1.0	Official release	2019/10/21

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1 MemxPro Memory Product Description

1.1 Introduction

MemxPro Small Outline DDR4 VLP ECC UDIMMs are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These DDR4 VLP ECC UDIMMs are intended for use as main memory when installed in systems such as micro servers and mobile personal computers.

1.2 Key Parameter

Industry Nomenclature	Data Rate MT/s		tRCD (ns)	tRP (ns)
	CL=17	CL=19		
PC4-21300	2400	2666	13.75	13.75

1.3 Ordering Information

DDR4 ECC UDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	Operating temperature
D4Q-AG26H1G8C2	16GB	PC4-21300	2Gx72	18	2	0°C to 85°C
D4Q-AG26H1G8E2	16GB	PC4-21300	2Gx72	18	2	-25°C to 85°C
D4Q-AG26H1G8W2	16GB	PC4-21300	2Gx72	18	2	-40°C to 85°C

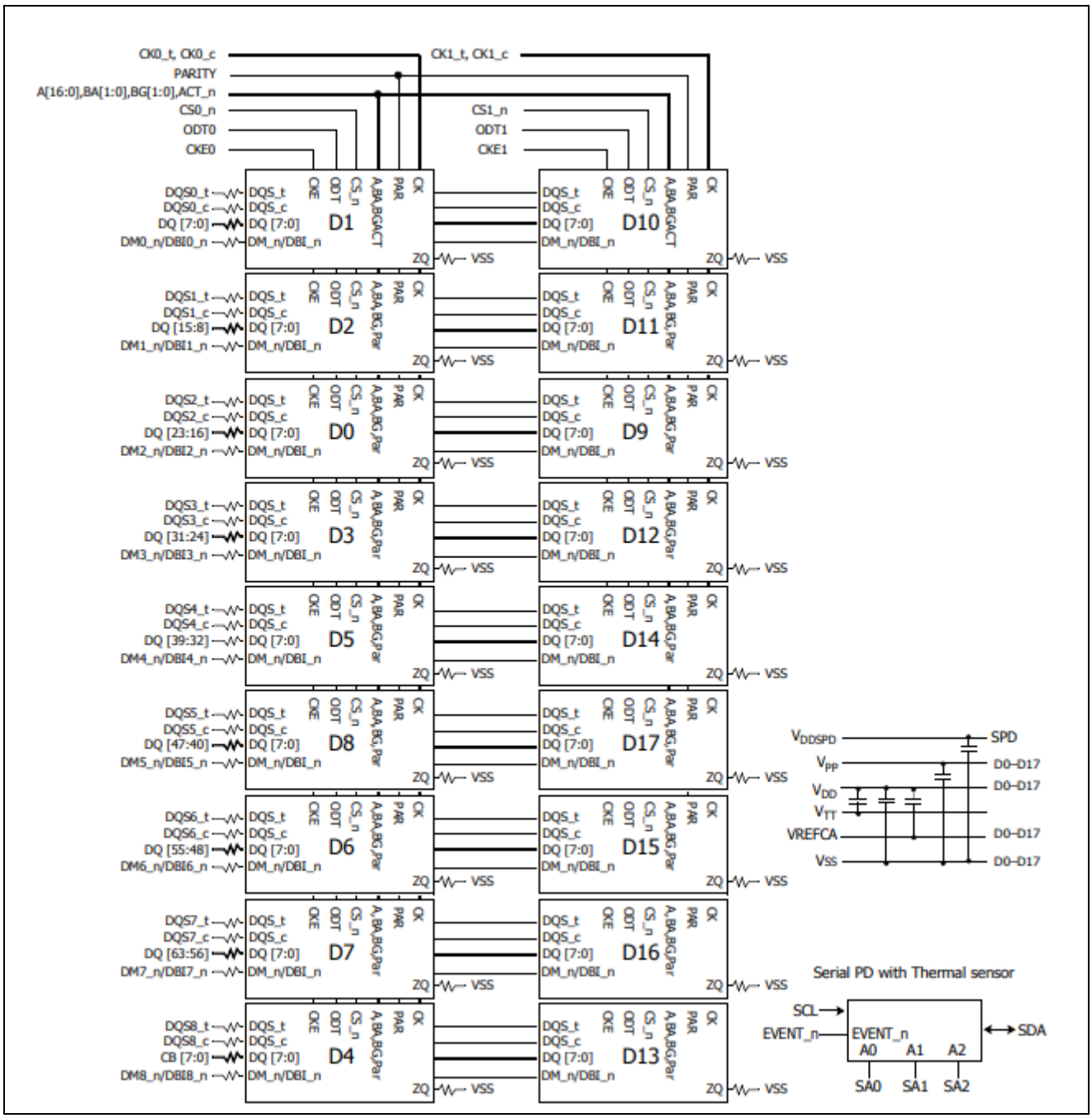
1.4 Memxpro Value Added Service

Memxpro DIMM provides specialized services to IPC designing customized hardware and systems by offering:

- Locked BOM control with customer product change notification(PCN)
- Pre-installed software, custom software imaging and ID strings
- Custom packaging and labeling
- Comprehensive supply-chain management
- Customer specified testing
- Localized Field Application Engineering for complete pre and post-sale technical support
- Optional Extend Temperature, ASTM B809-95 certified and conformal coating service.

2 Memxpro Memory Module Block Diagram

DDR4,16GB, 1Gx8 base, 2Rank



Note:

- Unless otherwise noted, resistor value are 15Ω±5%
- ZQ resisters are 240Ω±1%. For all other resistor values refer to the appropriated wiring diagram
- To connector the SPDA2 input to the edge connector pin 166 install R1. To tie the SPD input A2 to ground install R2. Do not install both R1 and R2. The Value for R1 and R2 are not critical. Any value less than 100Ω may be used.

3 Environment Requirement

3.1 Memxpro DIMM Parameter

Memxpro DIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TSTG	Storage Temperature	-50 to +100	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	
PBAR	Barometric Pressure (operating& storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in theDDR4 DRAM component specification.
2. Up to 9850 ft.

3.2 SDARM parameter by device density

RTT_Nom Setting	Parameter		4Gb	Units
tREFI	Average periodic refresh interval	0°C≤TCASE≤85°C	7.8	µs
		85°C≤TCASE≤95°C	3.9	µs

4 Absolute Maximum Rating

4.1 Module Absolut Maximum Rating

Symbol	Parameter	Rating	Units	Notes
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.4 to 1.5	V	
V_{DD}	Voltage on VDD supply relative to Vss	-0.4 to +1.5	V	1
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.4 to +1.5	V	1
V_{PP}	Voltage on VPP supply relative to Vss	-0.4 to +3.0	V	2

Note:
1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.

4.2 SDRAM Absolut Maximum Rating

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Standard	0 to 85	°C	1,2
		Extended	-25 to 85	°C	1,2
		Industrial	-40 to 85	°C	1,2
T_{STG}	Storage Temperature		-55 to 100	°C	3,4
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	3
V_{DD}	Voltage on V_{DD} supply relative to Vss		-0.3 to +1.5	V	3,5
V_{DDQ}	Voltage on V_{DDQ} supply relative to Vss		-0.3 to +1.5	V	3,5

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C underall operating conditions.
   - 2.1 Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   - 2.2 If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
3. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurementconditions, please refer to JESD51-2 standard.
5. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

5 Pin Configurations (Front side/Back side)

5.1 DDR4 VLP ECC UDIMM Pin Assignment

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	NC	145	NC	74	CK0_t	218	CK1_t
2	VSS	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	VSS	76	VDD	220	VDD
4	VSS	148	DQ5	77	VTT	221	VTT
5	DQ0	149	VSS	KEY			
6	VSS	150	DQ1				
7	DM0_n, DBI0_n, NC	151	VSS	78	EVENT_n	222	PARITY
8	NC	152	DQS0_c	79	A0	223	VDD
9	VSS	153	DQS0_t	80	VDD	224	BA1
10	DQ6	154	VSS	81	BA0	225	A10/AP
11	VSS	155	DQ7	82	RAS_n/A16	226	VDD
12	DQ2	156	VSS	83	VDD	227	RFU
13	VSS	157	DQ3	84	CS0_n	228	WE_n/A14
14	DQ12	158	VSS	85	VDD	229	VDD
15	VSS	159	DQ13	86	CAS_n/A15	230	NC
16	DQ8	160	VSS	87	ODT0	231	VDD
17	VSS	161	DQ9	88	VDD	232	A13
18	DM1_n, DBI1_n, NC	162	VSS	89	CS1_n	233	VDD
19	NC	163	DQS1_c	90	VDD	234	NC
20	VSS	164	DQS1_t	91	ODT1	235	NC
21	DQ14	165	VSS	92	VDD	236	VDD
22	VSS	166	DQ15	93	NC	237	NC
23	DQ10	167	VSS	94	VSS	238	SA2
24	VSS	168	DQ11	95	DQ36	239	VSS
25	DQ20	169	VSS	96	VSS	240	DQ37
26	VSS	170	DQ21	97	DQ32	241	VSS
27	DQ16	171	VSS	98	VSS	242	DQ33
28	VSS	172	DQ17	99	DM4_n, DBI4_n, NC	243	VSS
29	DM2_n, DBI2_n, NC	173	VSS	100	NC	244	DQS4_c
30	NC	174	DQS2_c	101	VSS	245	DQS4_t
31	VSS	175	DQS2_t	102	DQ38	246	VSS
32	DQ22	176	VSS	103	VSS	247	DQ39
33	VSS	177	DQ23	104	DQ34	248	VSS
34	DQ18	178	VSS	105	VSS	249	DQ35
35	VSS	179	DQ19	106	DQ44	250	VSS
36	DQ28	180	VSS	107	VSS	251	DQ45
37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
39	VSS	183	DQ25	110	DM5_n, DBI5_n, NC	254	VSS
40	DM3_n, DBI3_n, NC	184	VSS	111	NC	255	DQS5_c
41	NC	185	DQS3_c	112	VSS	256	DQS5_t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4, NC	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5, NC	119	DQ48	263	VSS
49	CB0, NC	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1, NC	121	DM6_n, DBI6_n, NC	265	VSS
51	DM8_n, DBI8_n, NC	195	VSS	122	NC	266	DQS6_c
52	NC	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS
54	CB6, NC	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7, NC	126	DQ50	270	VSS
56	CB2, NC	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3, NC	128	DQ60	272	VSS
58	RESET_n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1	130	DQ56	274	VSS
60	CKE0	204	VDD	131	VSS	275	DQ57
61	VDD	205	RFU	132	DM7_n, DBI7_n, NC	276	VSS
62	ACT_n	206	VDD	133	NC	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT_n	135	DQ62	279	VSS
65	A12/BC_n	209	VDD	136	VSS	280	DQ63
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59
68	A8	213	VDD	139	SA0	283	VSS
69	A6	214	A5	140	SA1	284	VDDSPD
70	VDD	215	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
72	A1	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

5.2 Pin Description

Pin Name	Description	Pin Name	Description
A0-A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0-SA2	I^2C slave address select for SPD/TS
RAS_n[1]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[2]	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n[3]	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CEK1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0-CB7	DIMM ECC check bits		
DQS0_t-DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c-DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred
DM0_n-DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	VTT	Termination supply for the Address, Command and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

1. RAS_n is a multiplexed function with A16.
2. CAS_n is a multiplexed function with A15.
3. WE_n is a multiplexed function with A14.

6 Memxpro SDRAM Operation Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/address bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3
I_{VTT}	Termination reference voltage (DC) – command/address bus	-750	-	750	mA	
V_{TT}	Termination Voltage	0.49 × VDD - 20mV	0.5 × VDD	0.51 × VDD + 20mV	V	4
I_I	Input leakage current; any input excluding ZQ; 0V < VIN < 1.1V	-2.0	-	2.0	µA	5
II/O	DQ leakage; 0V < Vin < VDD	-4.0	-	4.0	µA	5
I_{OZpd}	Output leakage current; VOUT = VDD; DQ is disabled	-	-	5.0	µA	5,6
I_{OZpu}	Output leakage current; VOUT =VSS; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	VREF + 0.125	-	VDDQ + 0.3	µA	1
I_{OZpd}	VREFCA leakage; VREFCA = VDD/2 (after DRAM is initialized)	-2.0	-	2.0	µA	5

Note:
1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
5. Multiply by the number of DRAM die on the module.
6. Tied to ground. Not connected to edge connector.

7 Operating, Standby and Refresh Currents

16GB VLP ECC UDIMM(1Gx8 2Rank DDR4 SDRAMs)

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IDD Max.	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	585	83	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	594	NA	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODTSignal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	675	92	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	702	NA	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheetfor detail pattern	504	58	mA

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IDD Max.	
IDD2NA	Precharge Standby Current (AL=CL-1)	504	NA	mA
	AL = CL-1, Other conditions: see IDD2N			
IDD2NT	Precharge Standby ODT Current	594	NA	mA
	CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to ComponentDatasheet for detail pattern			
IDD2NL	Precharge Standby Current with CAL enabled	378	NA	mA
	Same definition like for IDD2N, CAL enabled3			
IDD2NG	Precharge Standby Current with Gear Down mode enabled	504	NA	mA
	Same definition like for IDD2N, Gear Down mode enabled3			
IDD2ND	Precharge Standby Current with DLL disabled	486	NA	mA
	Same definition like for IDD2N, DLL disabled3			
IDD2N_par	Precharge Standby Current with CA parity enabled	504	NA	mA
	Same definition like for IDD2N, CA parity enabled3			
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;	360	58	mA
	Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0			
IDD2Q	Precharge Quiet Standby Current	450	NA	mA
	CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,			
	Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed;			
	Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0			

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IDD Max.	
IDD3N	Active Standby Current	684	270	mA
	CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,			
	Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks			
	open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet			
	for detail pattern			
IDD3NA	Active Standby Current (AL=CL-1)	684	NA	mA
	AL = CL-1, Other conditions: see IDD3N			
IDD3P	Active Power-Down Current	558	270	mA
	CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,			
	Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open;			
	Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0			
IDD4R	Operating Burst Read Current	1386	164	mA
	CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD;			
	Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different			
	data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through			
	banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to			
	Component Datasheet for detail pattern			

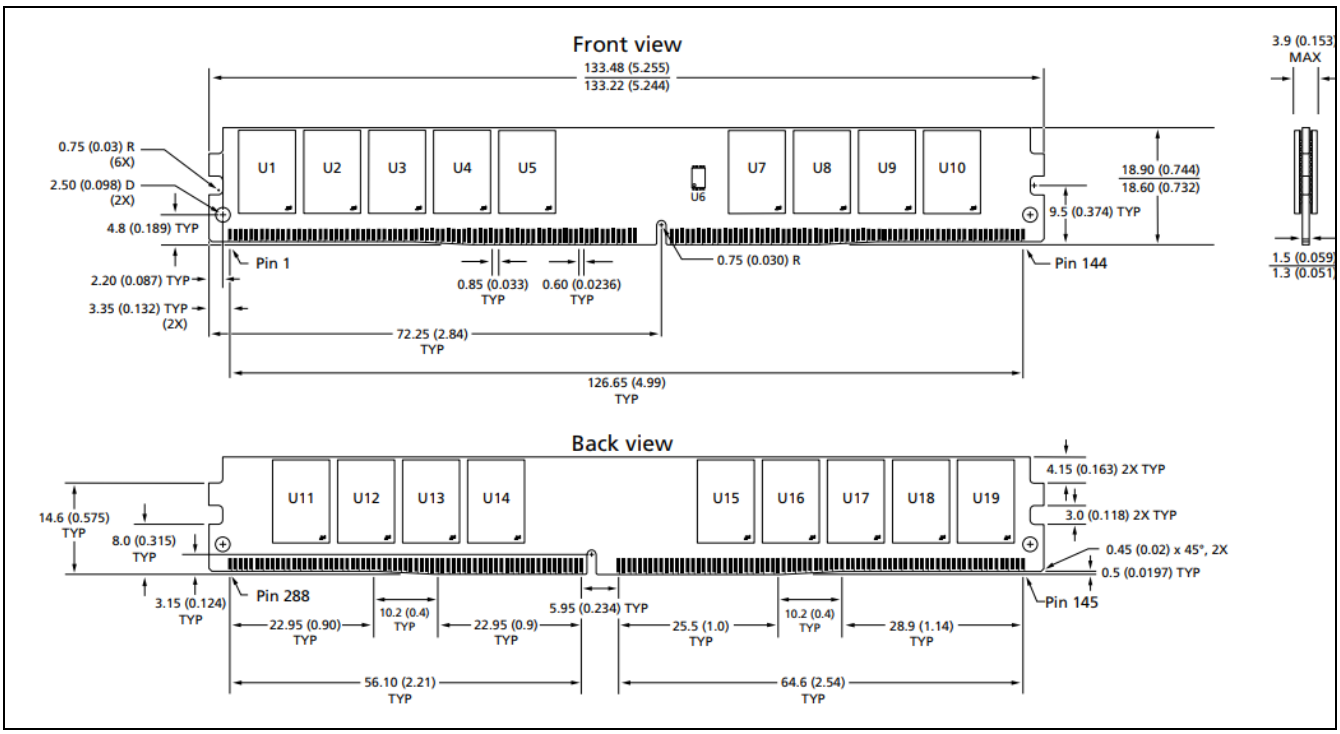
Symbol	Proposed Conditions	Value		Units
		IDD Max.	IDD Max.	
IDD4RA	Operating Burst Read Current (AL=CL-1)	1413	NA	mA
	AL = CL-1, Other conditions: see IDD4R			
IDD4RB	Operating Burst Read Current with Read DBI	1404	NA	mA
	Read DBI enabled3, Other conditions: see IDD4R			
IDD4W	Operating Burst Write Current	1224	164	mA
	CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR;			
	Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different			
	data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks:			
	0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component			
	Datasheet for detail pattern			
IDD4WA	Operating Burst Write Current (AL=CL-1)	1260	NA	mA
	AL = CL-1, Other conditions: see IDD4W			
IDD4WB	Operating Burst Write Current with Write DBI	1170	NA	mA
	Write DBI enabled3, Other conditions: see IDD4W			
IDD4WC	Operating Burst Write Current with Write CRC	1206	NA	mA
	Write CRC enabled3, Other conditions: see IDD4W			
IDD4W_par	Operating Burst Write Current with CA Parity	1377	NA	mA
	CA Parity enabled3, Other conditions: see IDD4W			

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IDD Max.	
IDD5B	Burst Refresh Current (1X REF)	2043	614	mA
	CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between			
	REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank			
	Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:			
	Refer to Component Datasheet for detail pattern			
IDD5F2	Burst Refresh Current (2X REF)	1575	443	mA
	tRFC=tRFC_x2, Other conditions: see IDD5B			
IDD5F4	Burst Refresh Current (4X REF)	1440	389	mA
	tRFC=tRFC_x4, Other conditions: see IDD5B			
IDD6N	Self Refresh Current: Normal Temperature Range	378	72	mA
	TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer			
	to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:			
	High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL			
IDD6E	Self-Refresh Current: Extended Temperature Range)	504	126	mA
	TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL:			
	Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data			
	IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode			
	Registers2; ODT Signal: MID-LEVEL			

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IDD Max.	
IDD6R	Self-Refresh Current: Reduced Temperature Range	252	74	mA
	TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW;			
	CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address,			
	Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode			
	Registers2; ODT Signal: MID-LEVEL			
IDD6A	Auto Self-Refresh Current	504	126	mA
	TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External			
	clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank			
	Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT:			
	Enabled in Mode Registers2; ODT Signal: MID-LEVEL			
IDD7	Operating Bank Interleave Read Current	1584	200	mA
	CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:			
	CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling			
	through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern			
	Details: Refer to Component Datasheet for detail pattern			
IDD8	Maximum Power Down Current TBD	216	58	mA

8 Package Dimension

8.1 16GB DDR4 VLP ECC UDIMM, 2Gx72, 2Rank



Note:

1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

9 Reliability Specifications

9.1 Environmental Conditions

Environment	Specification
Storage Temperature	-50°C ~ +100°C
Operating Temperature	0°C to 85°C (Standard); -25°C to 85°C (Extended) ;-40°C to 85°C (Industrial)
Vibration	20G
Shock	1000G@1ms

10 RoHS Declaration

MEMXPRO
Make it Possible

MemxPro-DIMM Declaration of Conformity

We, MemxPro Inc., here declare all MemxPro DRAM module products fully complied with the requirement of RoHS directives 2006/122/EC and RoHS Directive (2011/65/EU and 2015/863).

MemxPro Inc. ensures any MemxPro product meets RoHS requirements of ten restricted substances.
This declaration is based on qualified vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
Cadmium (Cd)	< 100 ppm
Lead (Pb)	< 1000 ppm
Mercury (Hg)	< 1000 ppm
Hexavalent chromium (Cr6+)	< 1000 ppm
Polybrominated biphenyls (PBB)	< 1000 ppm
Polybrominated diphenyl ethers (PBDE)	< 1000 ppm
Bis(2-ethylhexyl) phthalate (DEHP)	< 1000 ppm
Butyl benzyl phthalate (BBP)	< 1000 ppm
Dibutyl phthalate (DBP)	< 1000 ppm
Diisobutyl phthalate (DIBP)	< 1000 ppm
Perfluorooctane sulfonates (PFOS)	Not Contained

★ RoHS exemptions applied of 11(c)-I for resist.

Date Issue: 2018/01/01
Manufacturer: MemxPro Inc.
Address: 4F., NO.32, XIWEI ST., SANCHONG DIST.,
NEW TAIPEI CITY, 24155, TAIWA

Authorized Signature :

DRAM BU Manager – James Huang